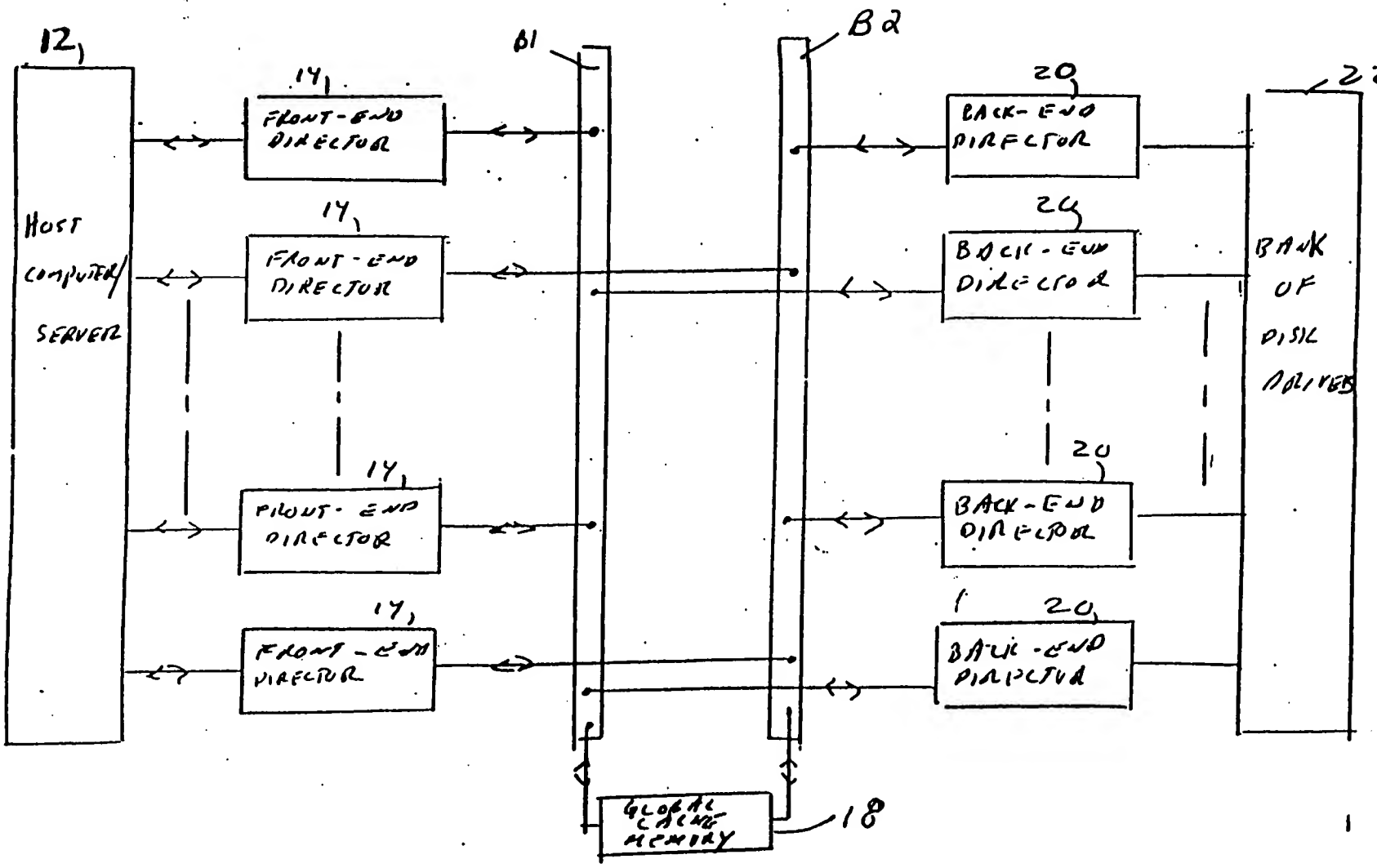
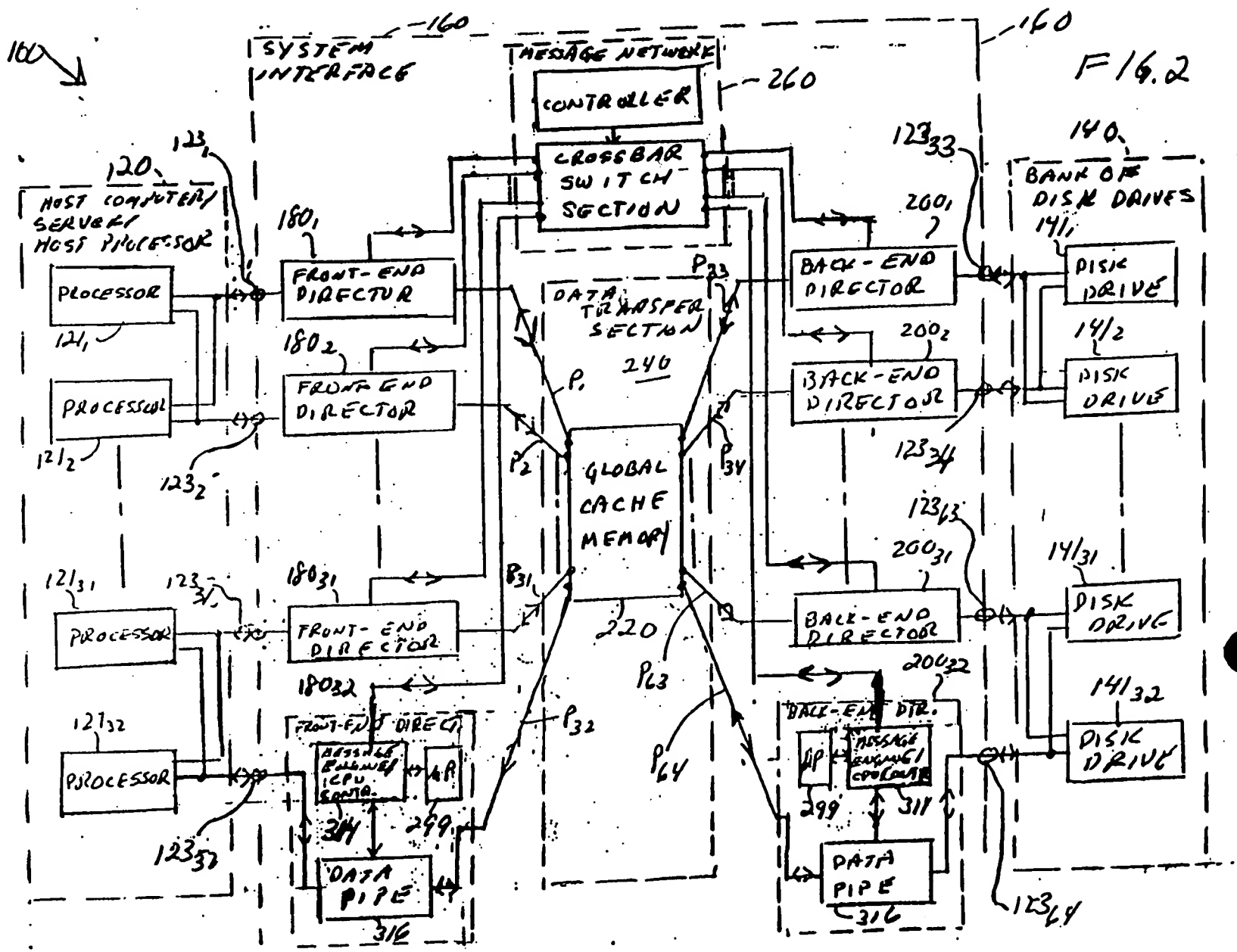
FIG. 1
PRIOR ART




100
160
SYSTEM INTERFACE
MESSAGE NETWORK
CONTROLLER
260
CROSSBAR SWITCH SECTION
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
PROCESSOR
121 1
121 2
121 31
121 32
123 1
123 2
123 31
123 32
180 1
180 2
180 31
180 32
FRONT-END DIRECTOR
DATA TRANSFER SECTION
240
P 1
P 2
P 31
P 32
GLOBAL CACHE MEMORY
220
P 33
P 34
P 63
P 64
200 1
200 2
200 31
200 32
BACK-END DIRECTOR
123 33
123 34
123 63
123 64
140
BANK OF DISK DRIVES
141 1
141 2
141 31
141 32
DISK DRIVE
299
311
316
DATA PIPE
MESSAGE ENGINE/ CPU
FIG. 2

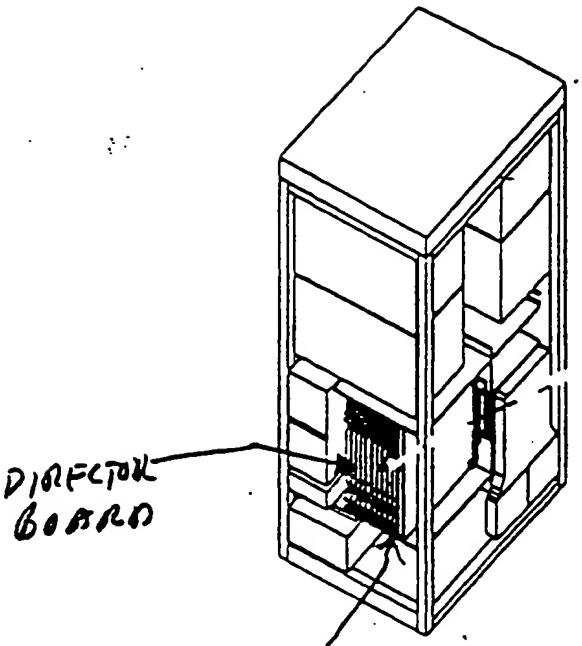
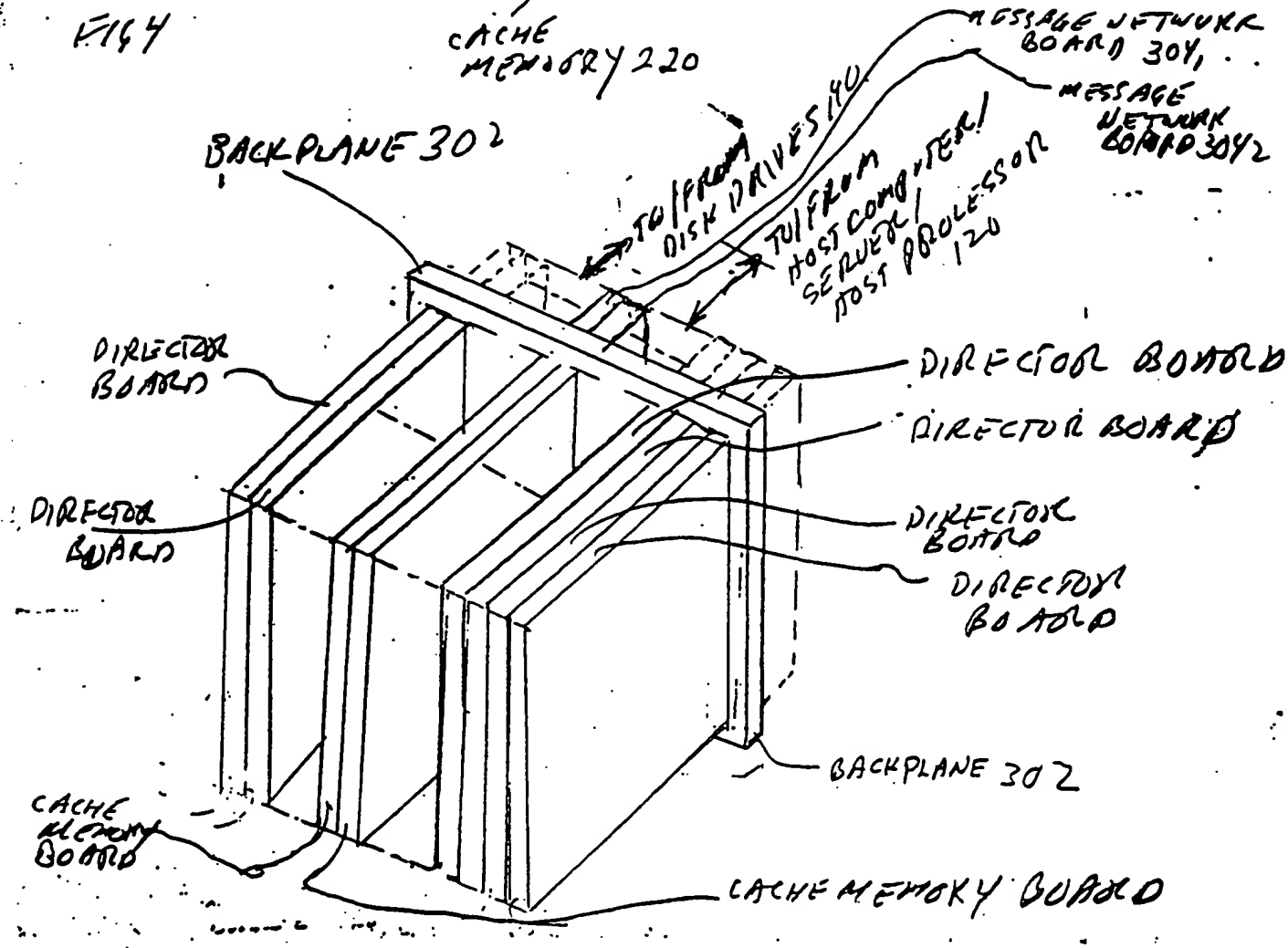
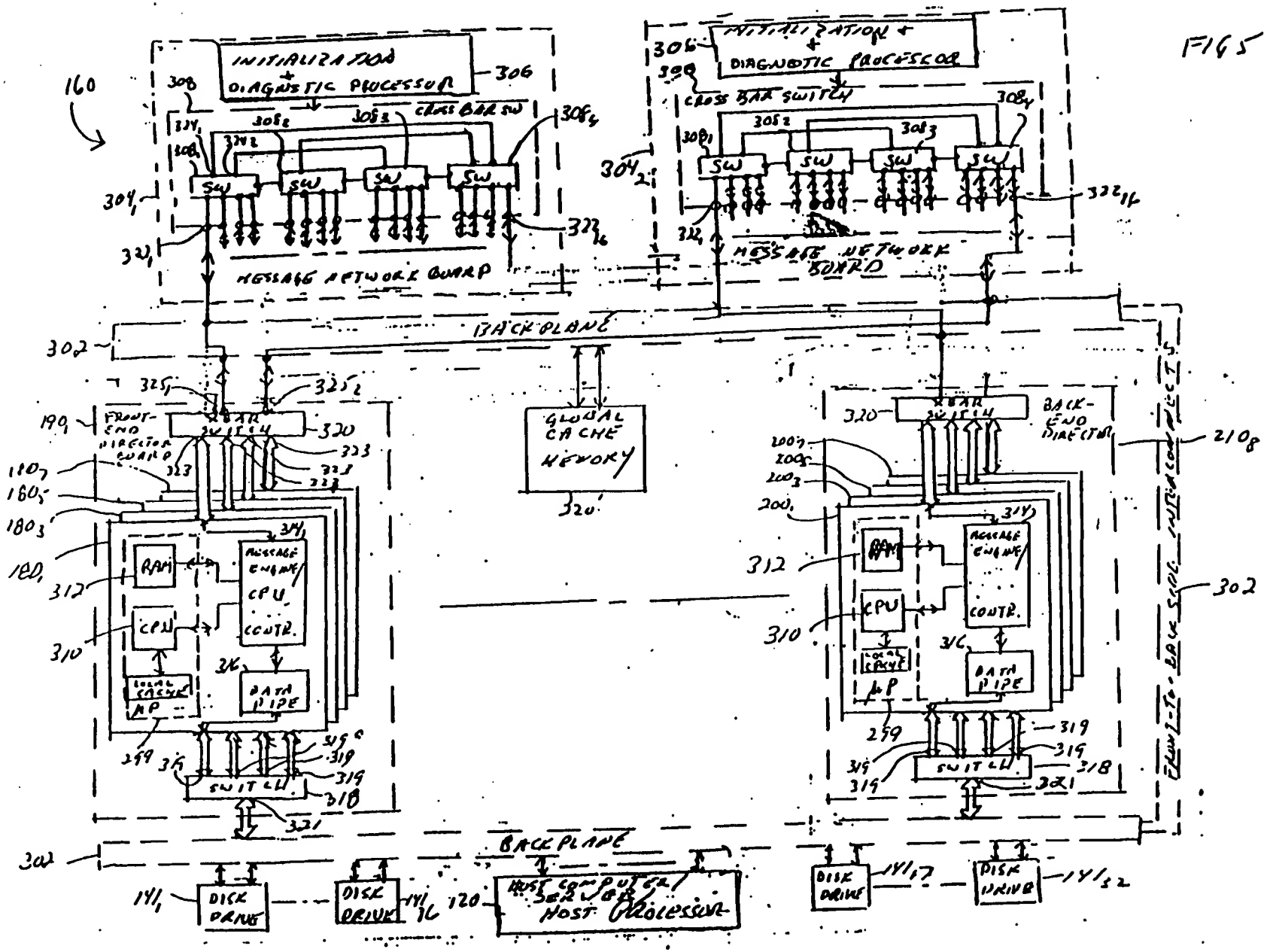

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304,
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD


160
INITIALIZATION + DIAGNOSTIC PROCESSOR
306
CROSS BAR SW
SW
MESSAGE NETWORK BOARD
MESSAGE NETWORK CARD
BACKPLANE
GLOBAL CACHE MEMORY
FRONT-END DIRECTOR CARD
BACK-END DIRECTOR
RAM
CPU
CONTR.
DATA PIPE
SWITCH
DISK DRIVE
HOST COMPUTER OR SERVER
FIG 5

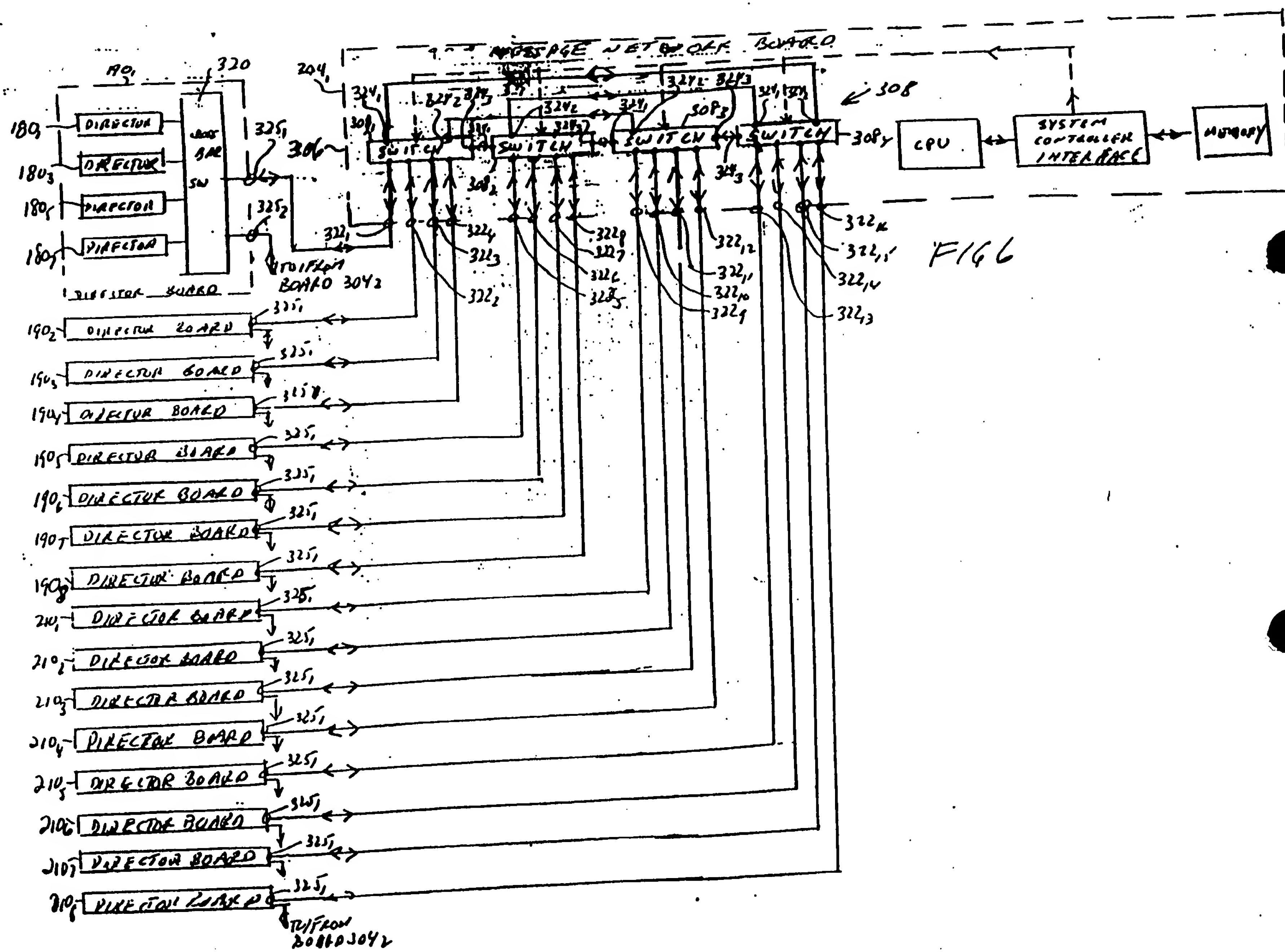
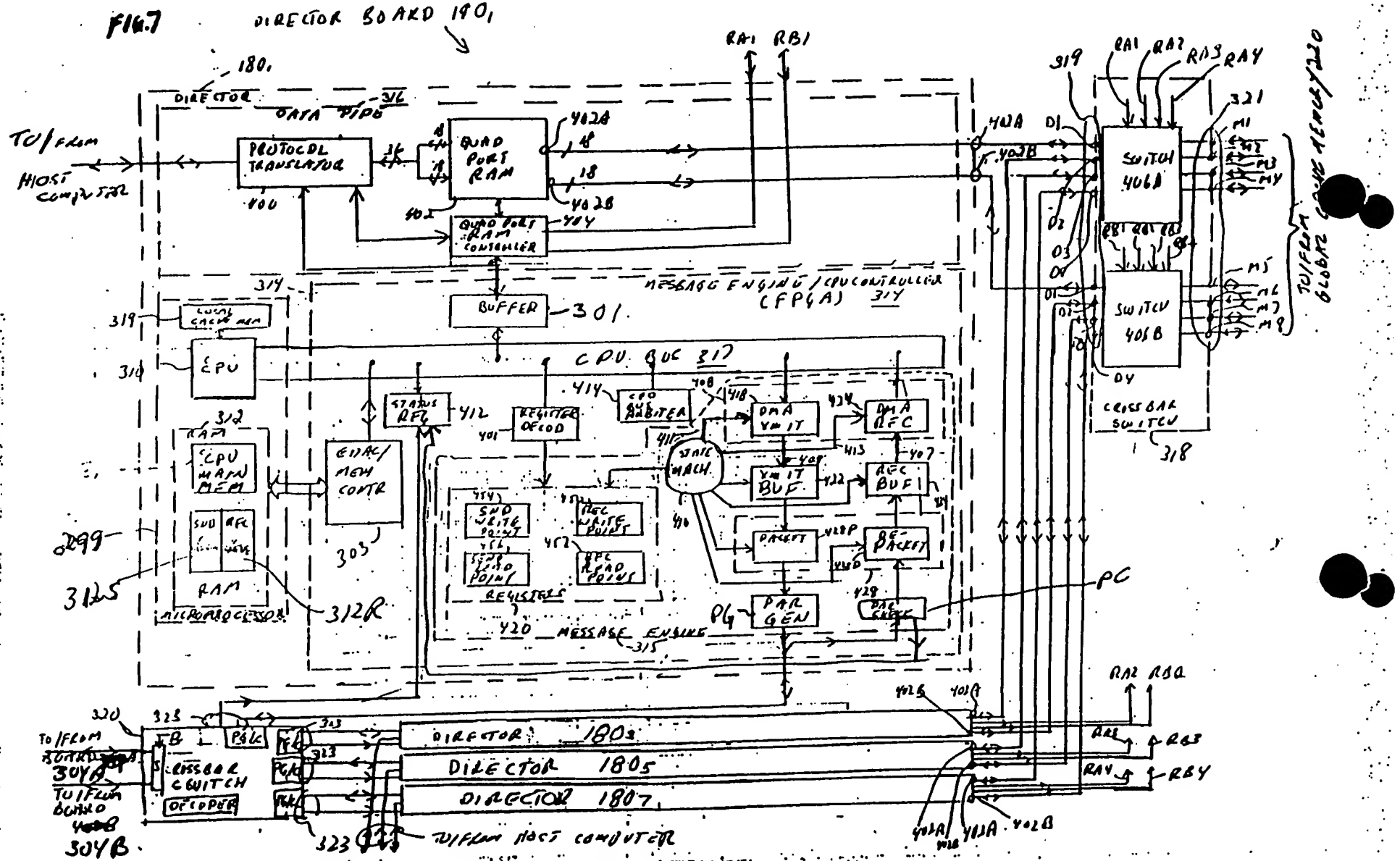


FIG 6

FIG. 7


DIRECTOR BOARD 190
180
DIRECTOR DATA PIPE
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
QUAD PORT RAM
QUAD PORT RAM CONTROLLER
BUFFER
MESSAGE ENGINE/CPU CONTROLLER (CPPGA)
LOCAL CACHE MEM
CPU
CPU BUS
STATUS REG
REGISTER DECOD
CPU ARBITER
DMA XMIT
DMA REC
STATE MACH.
XMIT BUF
REC BUF
PACKET
RE-PACKET
SND WRITE POINT
REC WRITE POINT
SEND READ POINT
REC READ POINT
REGISTERS
PAR GEN
PAR CHECK
MESSAGE ENGINE
CPU MAIN MEM
RAM
MICROPROCESSOR
EMAC/MEM CONTR
SWITCH 406A
SWITCH 406B
CROSSBAR SWITCH
TO/FROM GLOBAL CROSSBAR SWITCH
PC
DIRECTOR 1803
DIRECTOR 1805
DIRECTOR 1807
CROSSBAR SWITCH
DECODER
TO/FROM BOARD
TO/FROM HOST COMPUTER

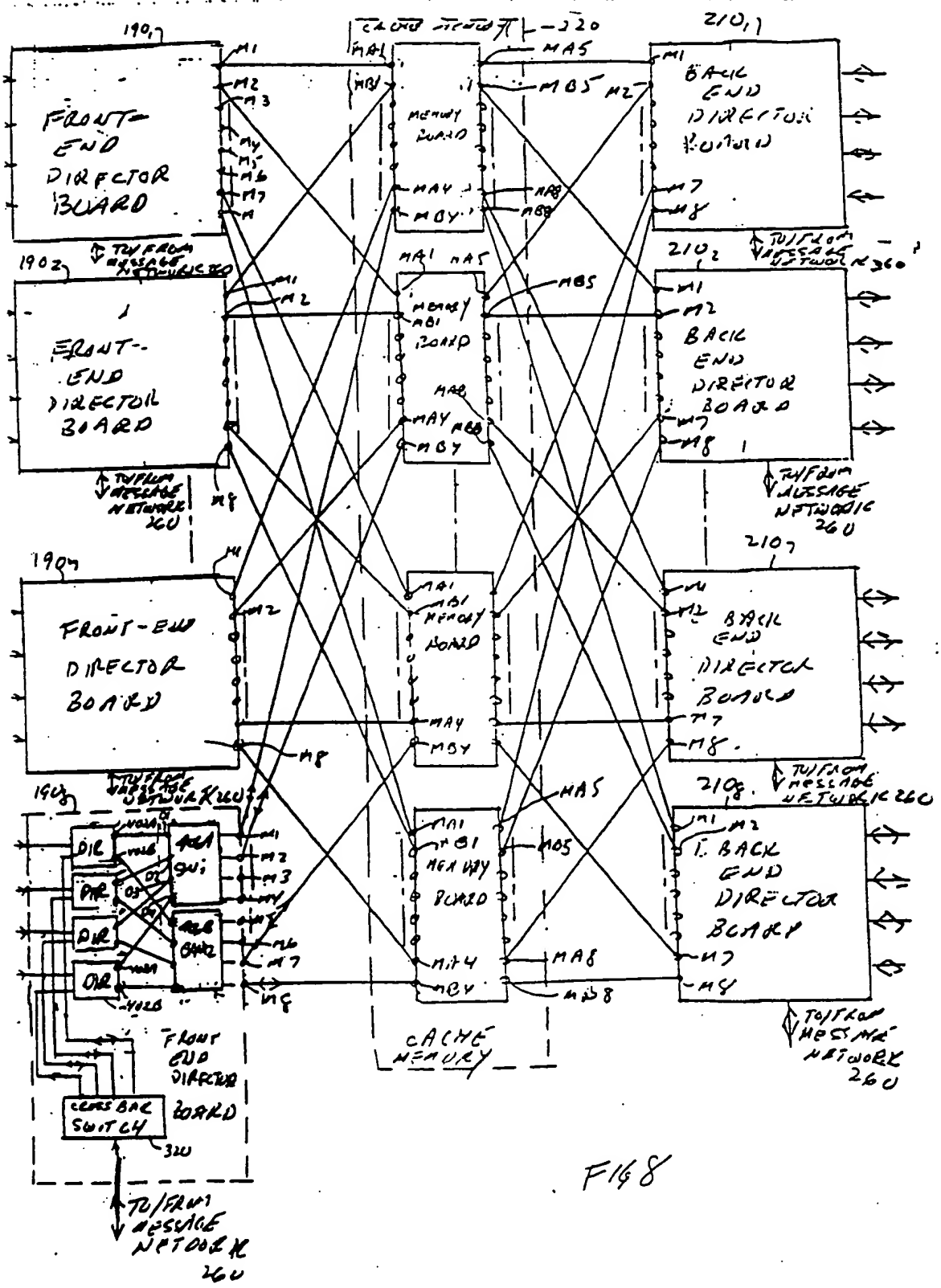
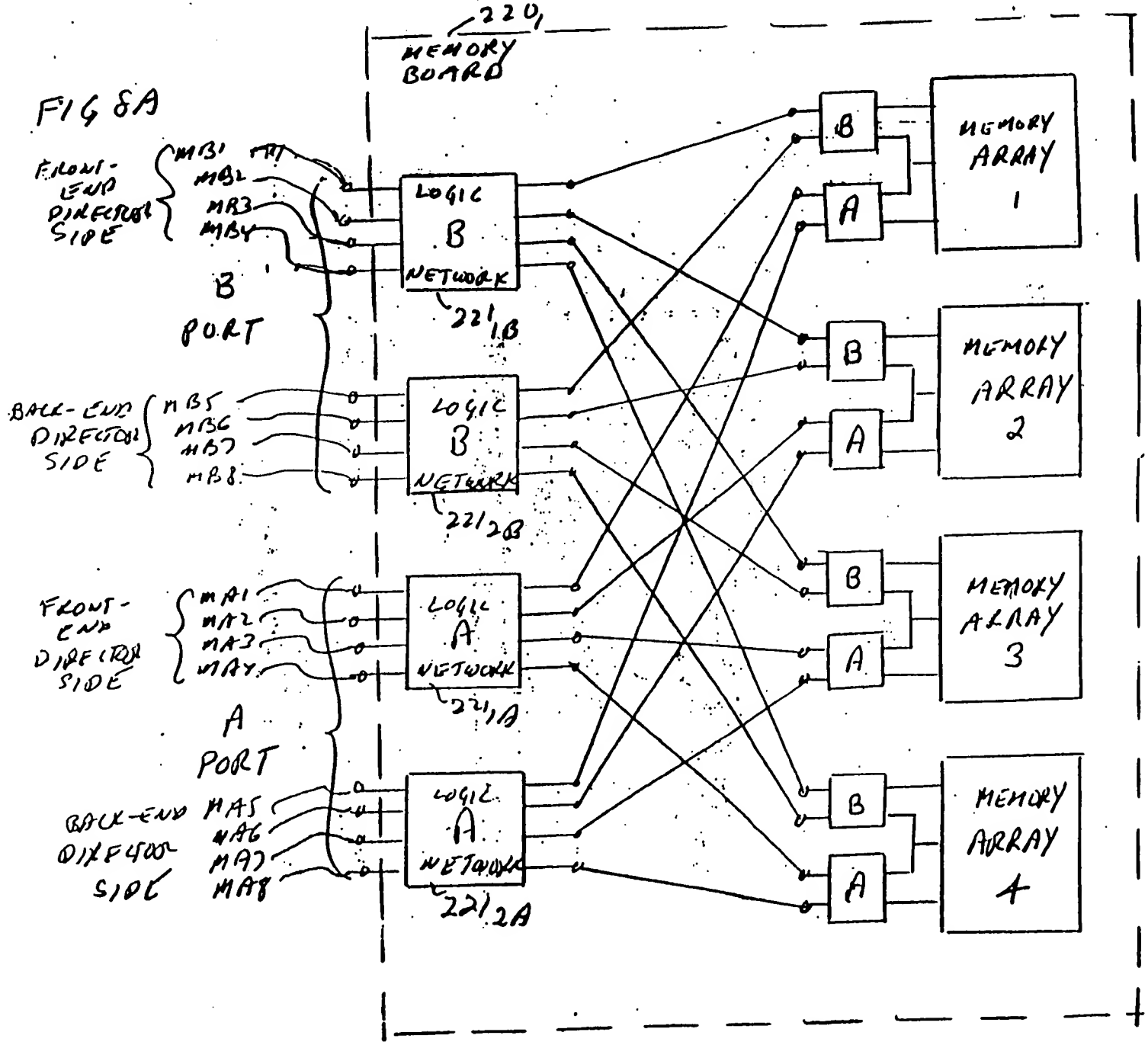

FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT END DIRECTOR BOARD
CROSS BAR SWITCH
MEMORY BOARD
MEMORY BOARD
MEMORY BOARD
MEMORY BOARD
CACHE MEMORY
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260

FIG 8

FIG 8A


220₁
MEMORY BOARD
FRONT-END DIRECTOR SIDE
MB1
MB2
MB3
MB4
B PORT
BACK-END DIRECTOR SIDE
MB5
MB6
MB7
MB8
FRONT-END DIRECTOR SIDE
MA1
MA2
MA3
MA4
A PORT
BACK-END DIRECTOR SIDE
MA5
MA6
MA7
MA8
LOGIC B NETWORK
221₁B
LOGIC B NETWORK
221₂B
LOGIC A NETWORK
221₁A
LOGIC A NETWORK
221₂A
B
A
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4

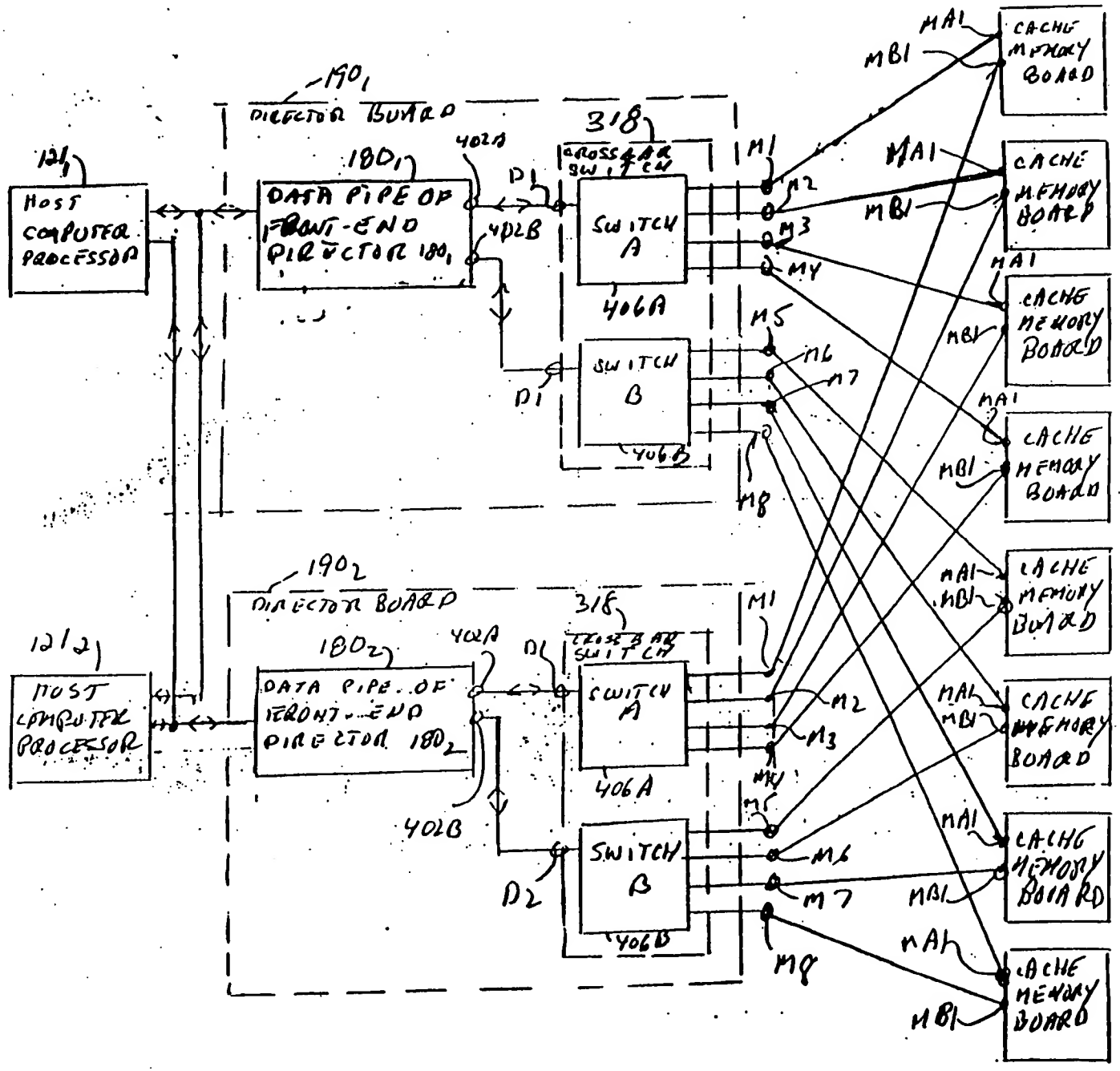

190₁
DIRECTOR BOARD
318
CROSSBAR SWITCH
121₁
HOST COMPUTER PROCESSOR
180₁
DATA PIPE OF FRONT-END DIRECTOR 180₁
402A
402B
D1
SWITCH A
406A
SWITCH B
406B
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
CACHE MEMORY BOARD
190₂
DIRECTOR BOARD
121₂
HOST COMPUTER PROCESSOR
180₂
DATA PIPE OF FRONT-END DIRECTOR 180₂
D2

FIG 8B

FIG. 8C

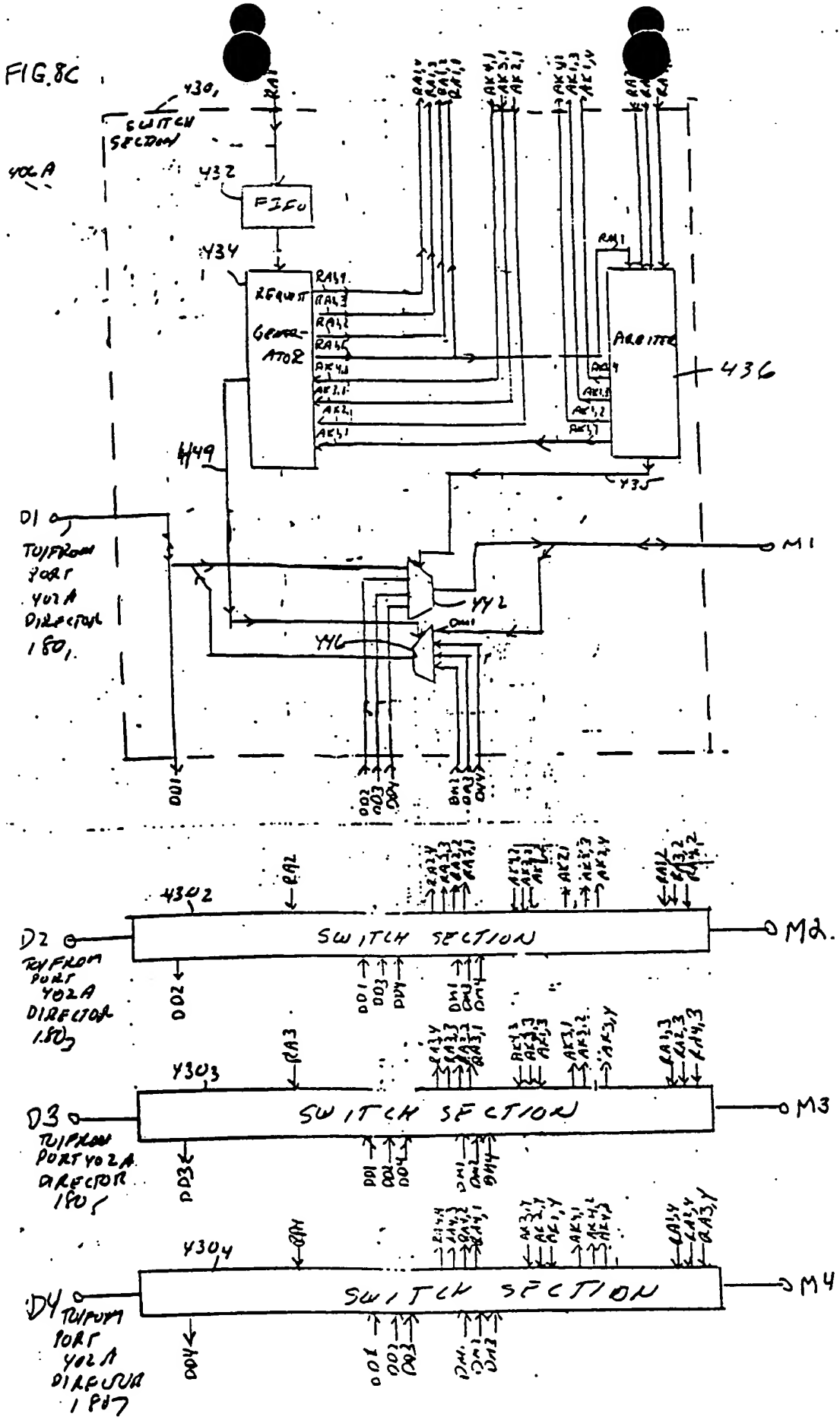

SWITCH SECTION
FIFO
REQUEST GENERATOR
ARBITER
SWITCH SECTION
SWITCH SECTION
SWITCH SECTION

FIG 9

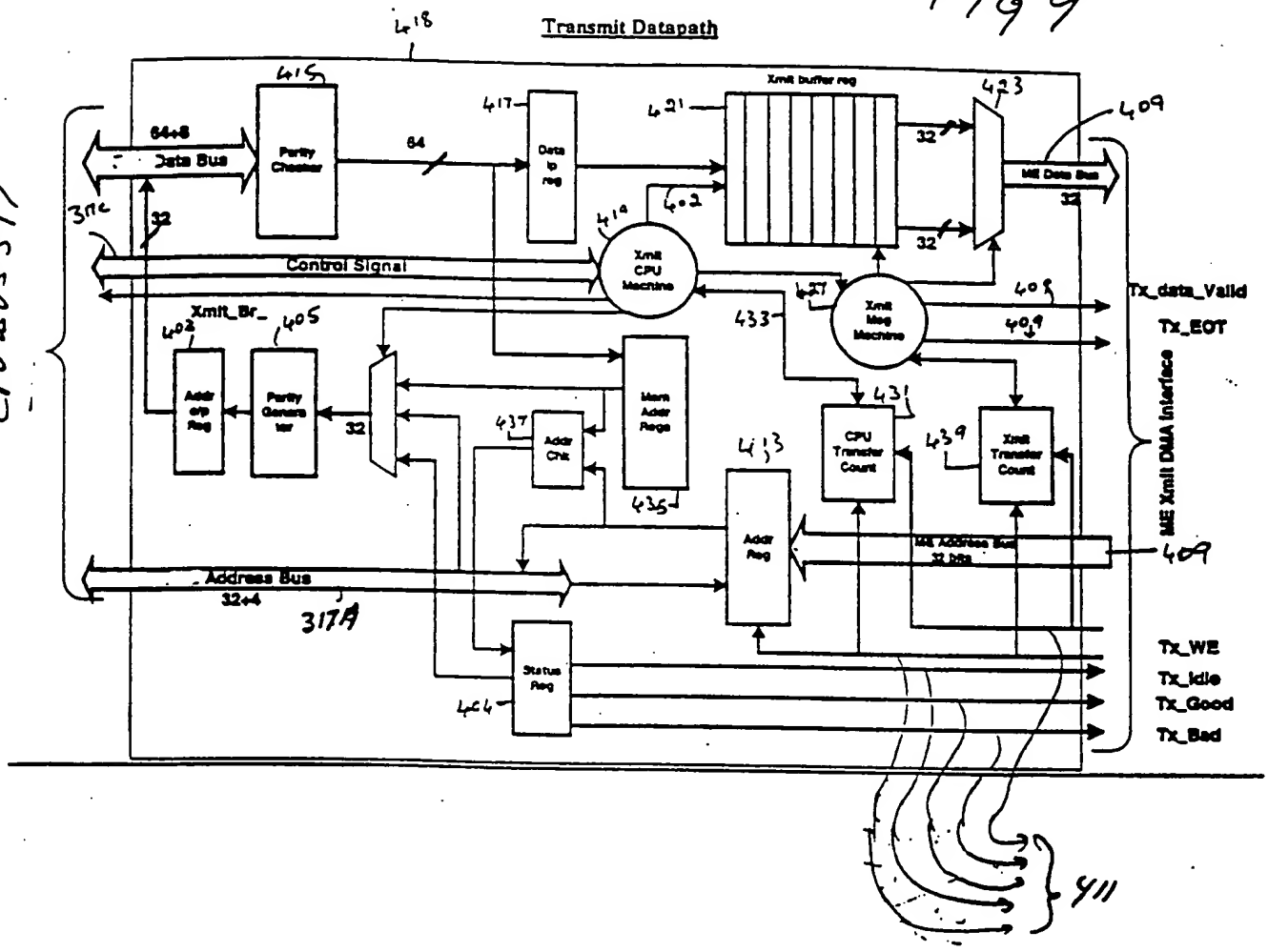

Transmit Datapath
418
415
417
421
423
409
64+8
Data Bus
Parity Checker
64
Data to reg
Xmit buffer reg
32
32
MII Data Bus
32
CPU BUS 317
32
Control Signal
414
402
Xmit CPU Machine
427
Xmit Msg Machine
433
409
409
Tx_data_Valid
Tx_EOT
Xmit_Br_
402
405
Addr o/p Reg
Parity Generator
32
Mem Addr Regs
437
Addr Chk
431
CPU Transfer Count
439
Xmit Transfer Count
MII Xmit DMA Interface
435
413
Addr Reg
MII Address Bus 32 bits
409
Address Bus
32+4
317A
Status Reg
404
Tx_WE
Tx_Idle
Tx_Good
Tx_Bad
411

FIG 10

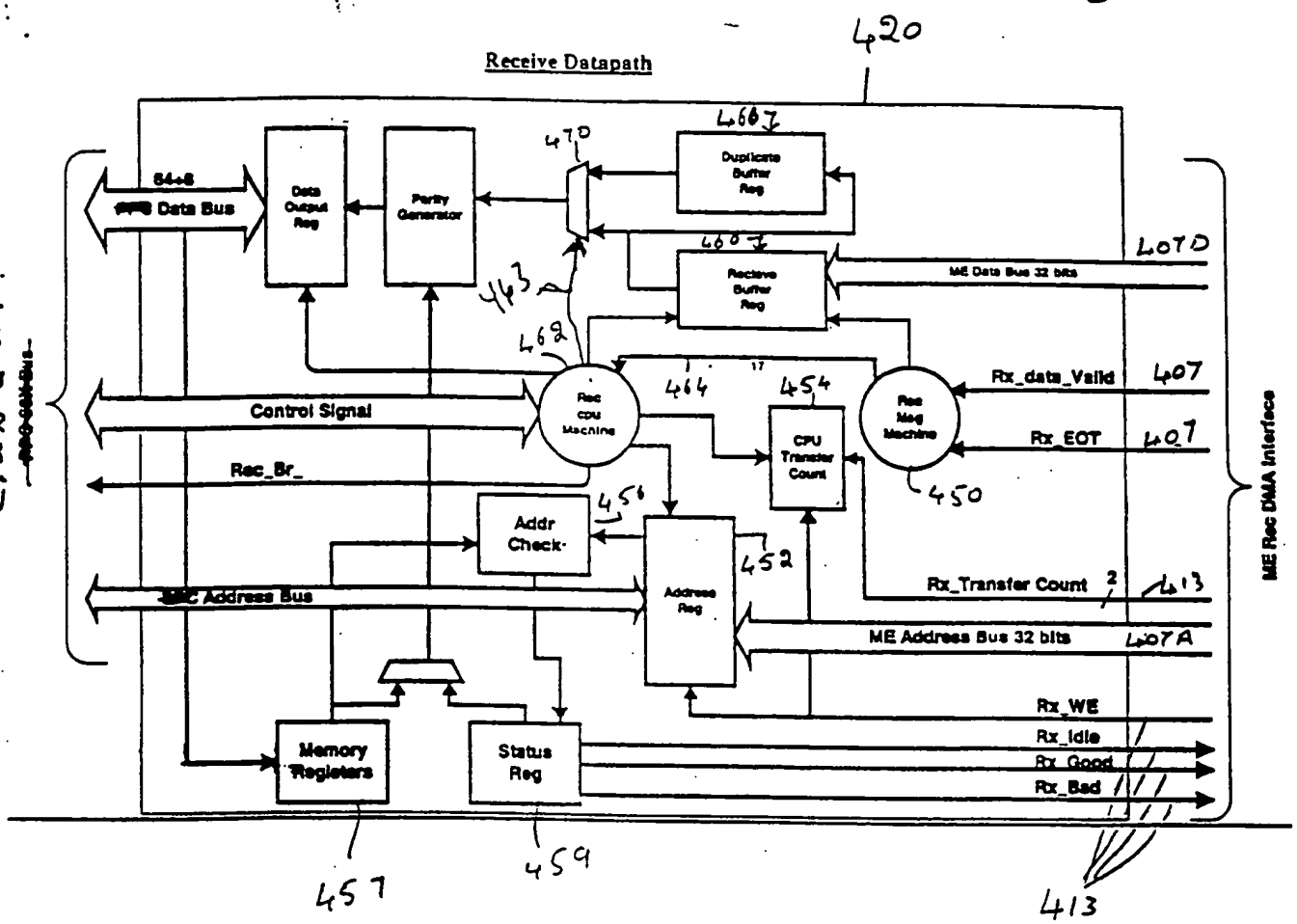

420
Receive Datapath
CPU BUS 317
64+8 Data Bus
Data Output Reg
Parity Generator
470
Duplicate Buffer Reg
460
Receive Buffer Reg
ME Data Bus 32 bits
405
463
462
Control Signal
Rec_Br_
Rec CPU Machine
464
17
454
CPU Transfer Count
Rec Msg Machine
Rx_data_Valid
Rx_EOT
407
450
Addr Check
456
452
Address Reg
Rx_Transfer Count
2
413
ME Address Bus 32 bits
407A
Rx_WE
Rx_Idle
Rx_Good
Rx_Bad
Memory Registers
Status Reg
457
459
413
ME Rec DMA Interface

FIG. 11A

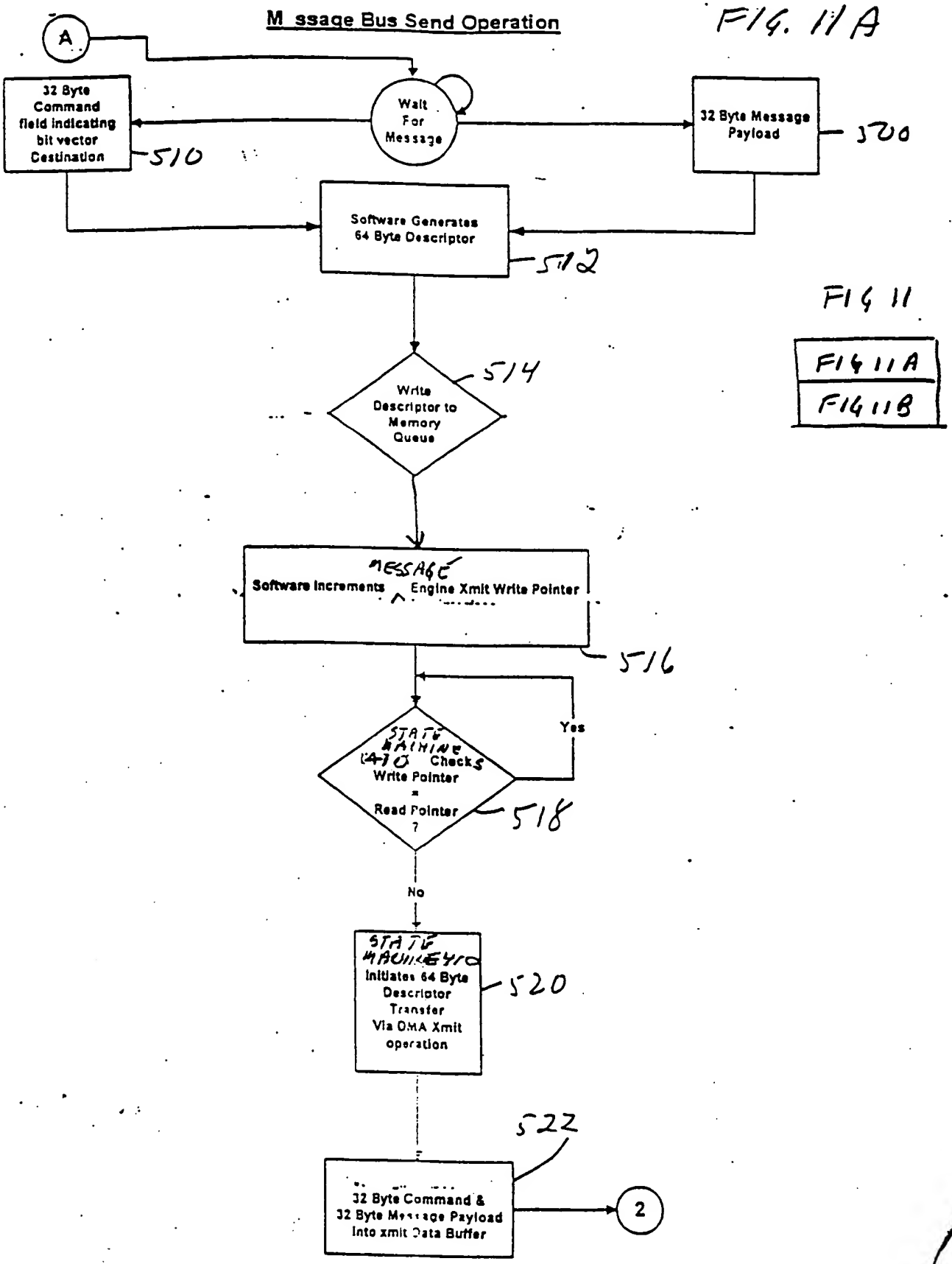
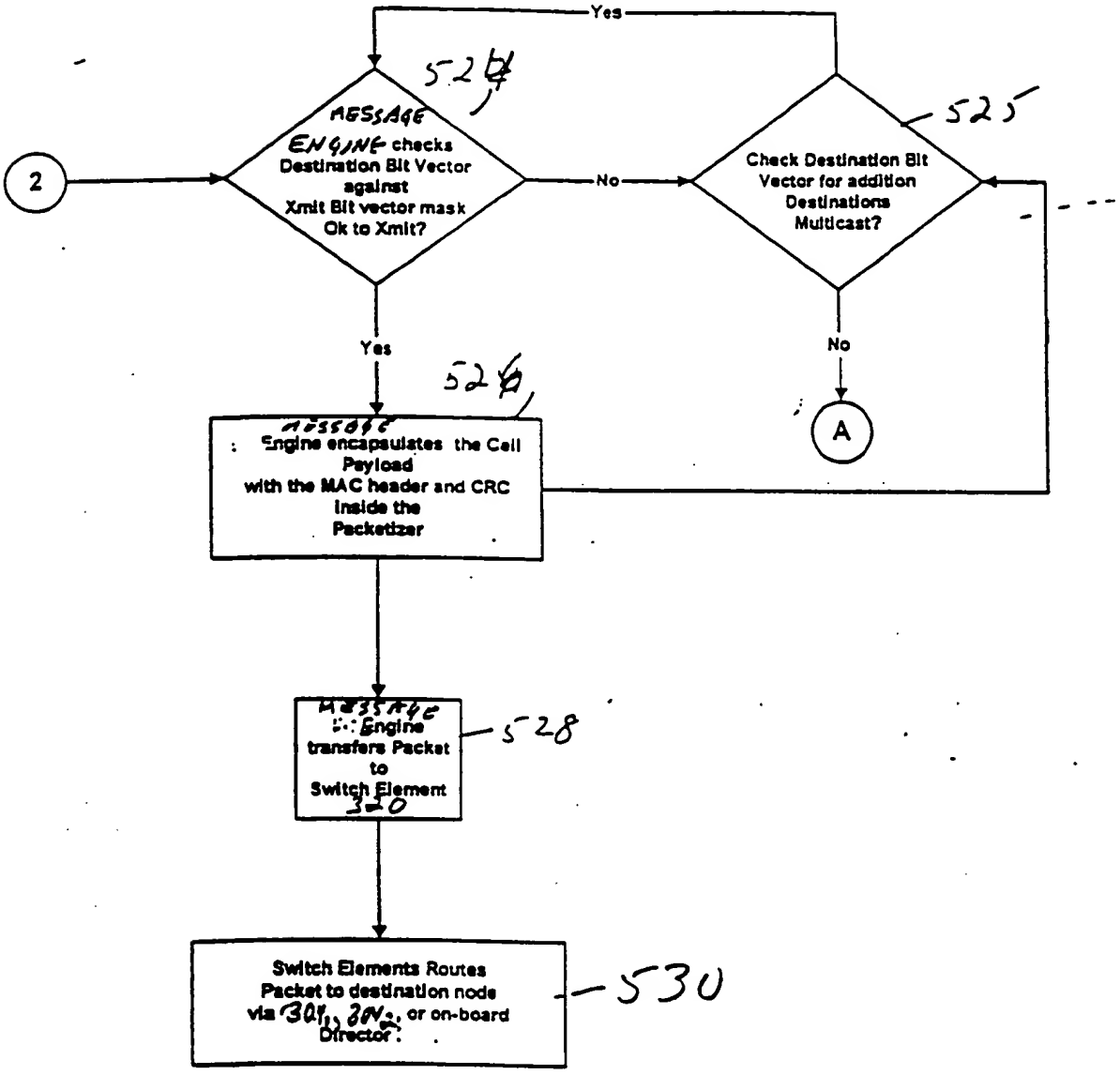


FIG 11

FIG 11A
FIG 11B

Message Bus Send Operation Continued

FIG 11B



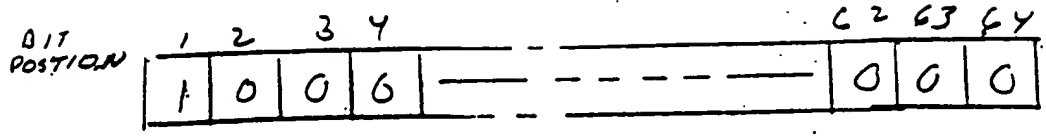


FIG 11C

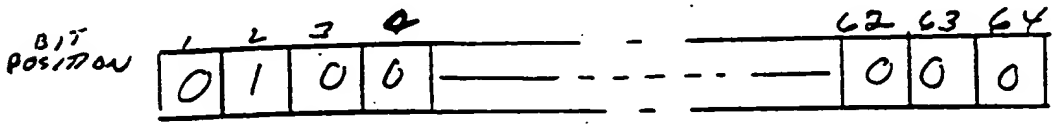


FIG 11D

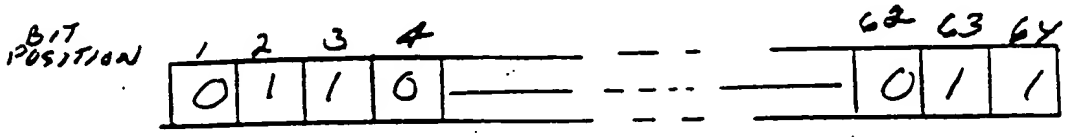


FIG 11E

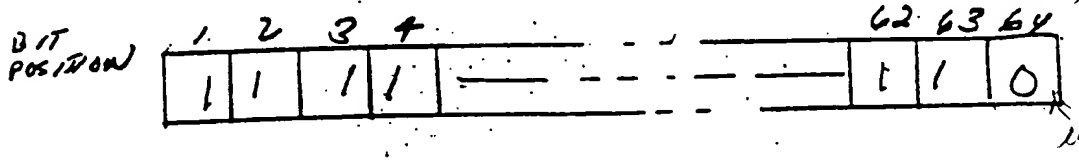


FIG 11F MMS

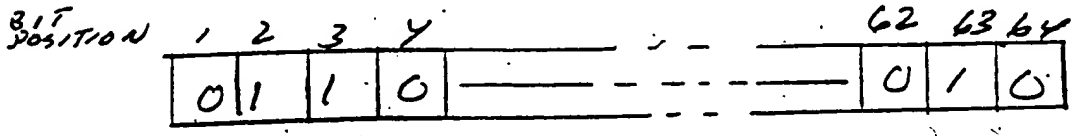


FIG 11G

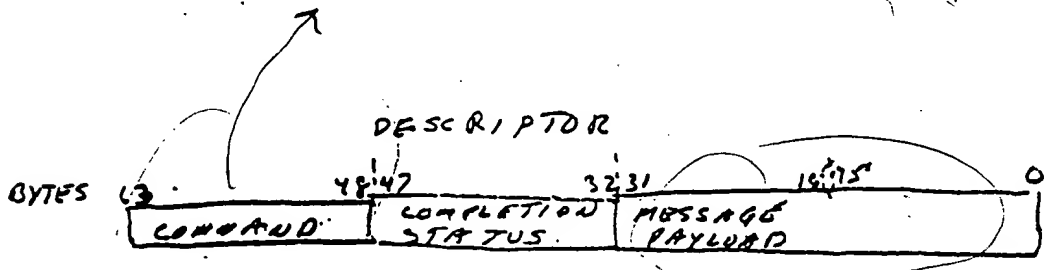


FIG 2A

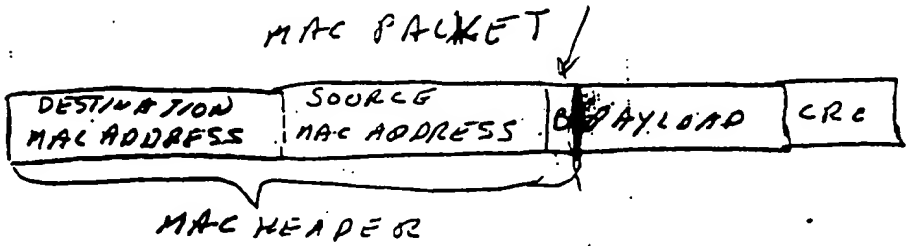


FIG 2B

Message Bus Receive Operation

FIG. 12A

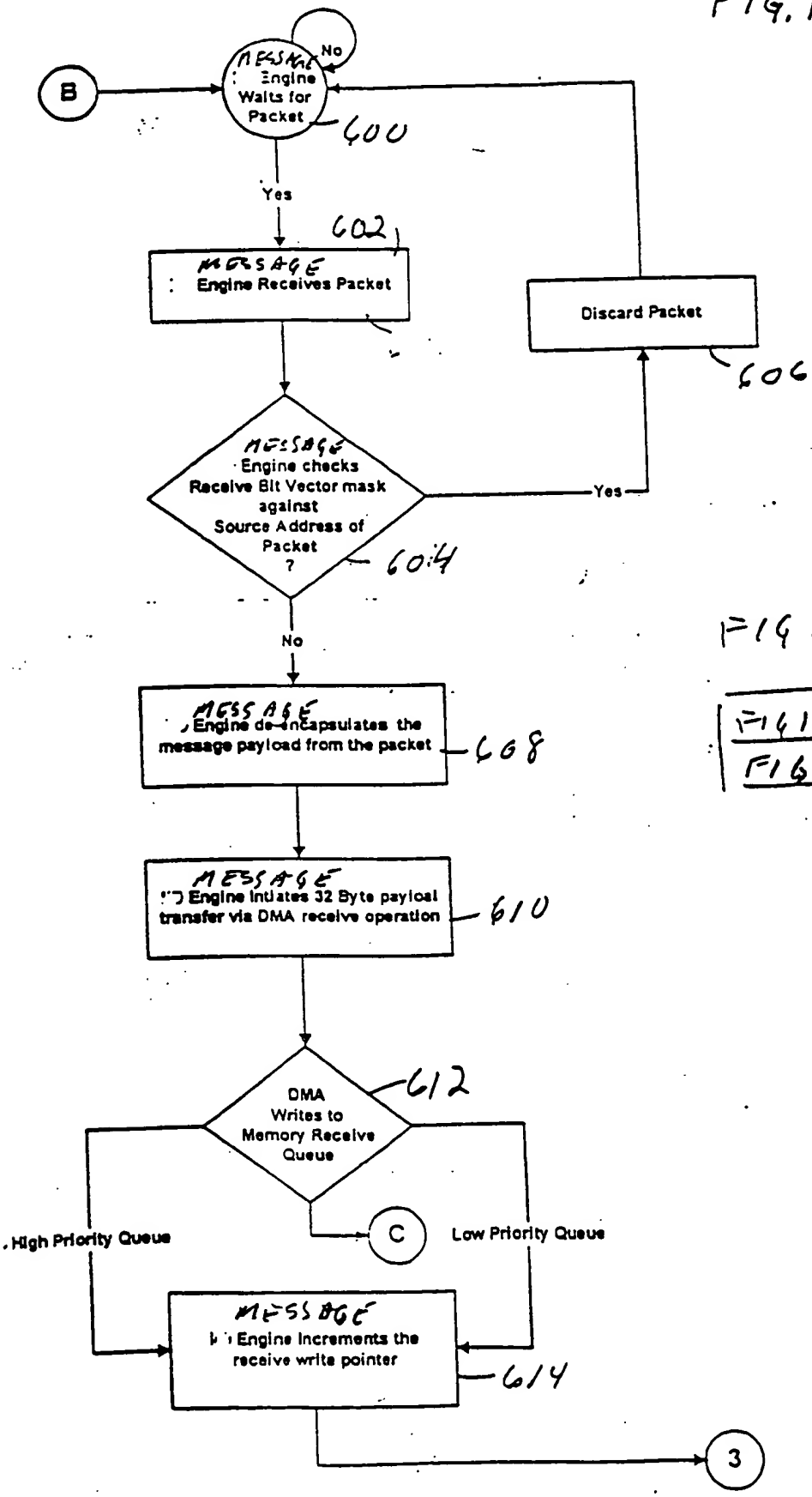


FIG 12

FIG 12A
FIG 12B

M sage Bus Receive Operation Continued

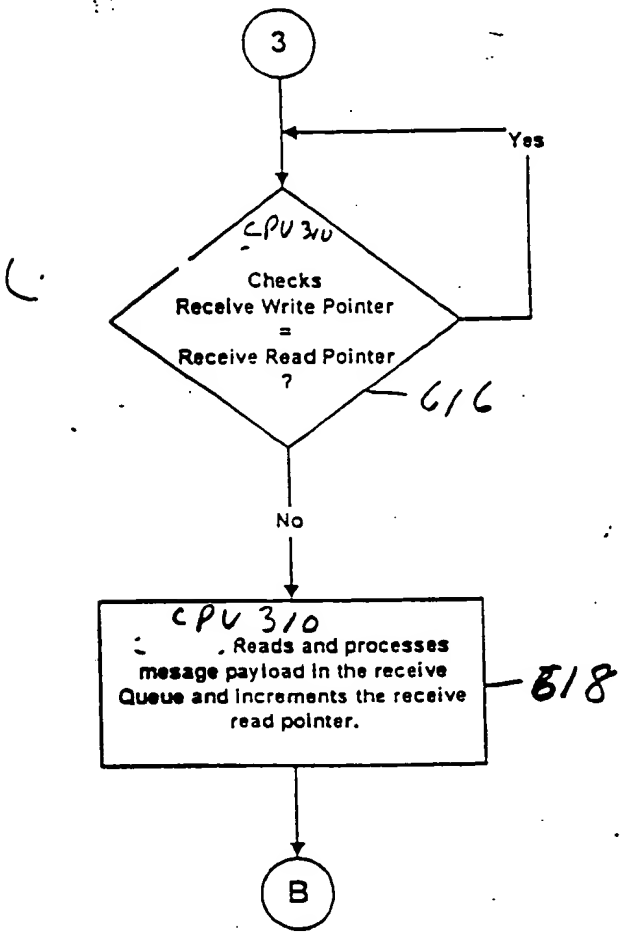


FIG 12B

Message Bus Acknowledg ment Operati n

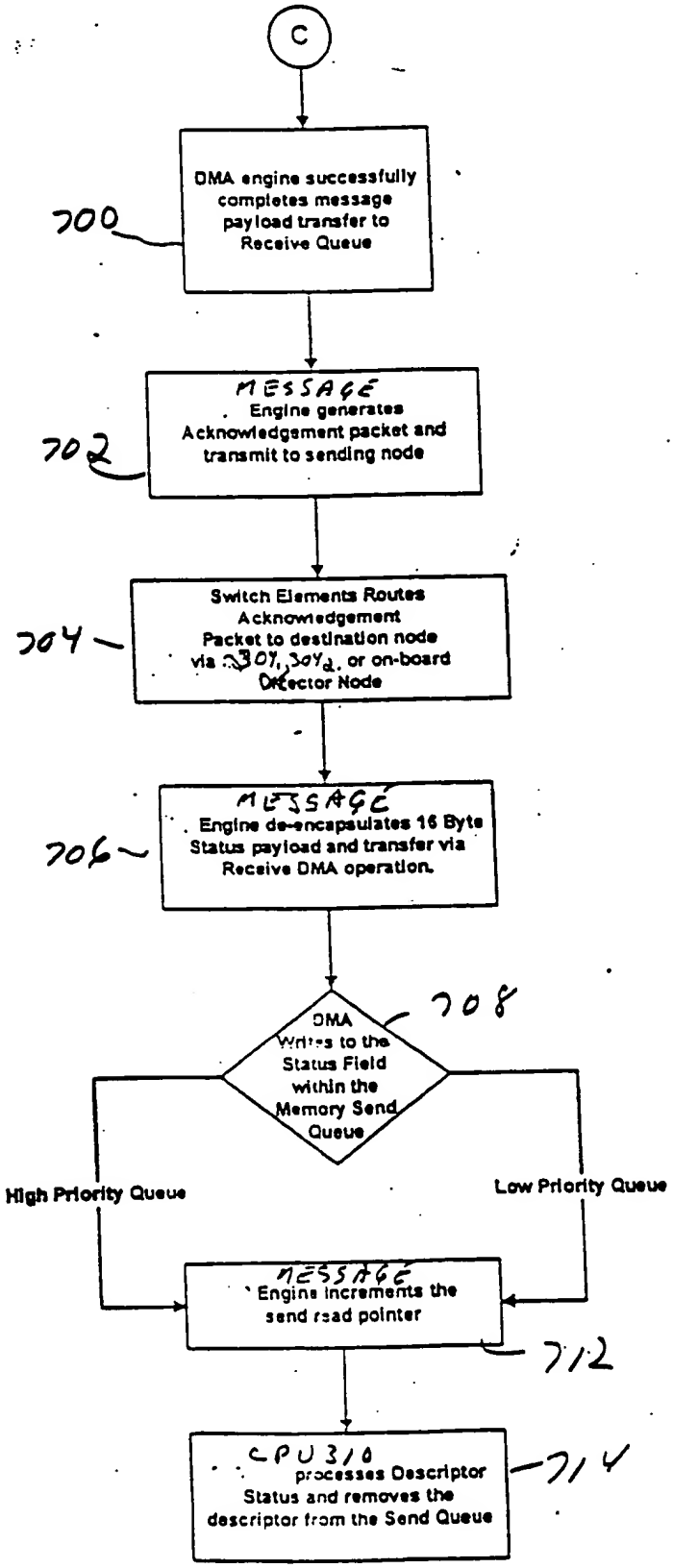


FIG. 13

FIG 4A

Xmit CPU flow

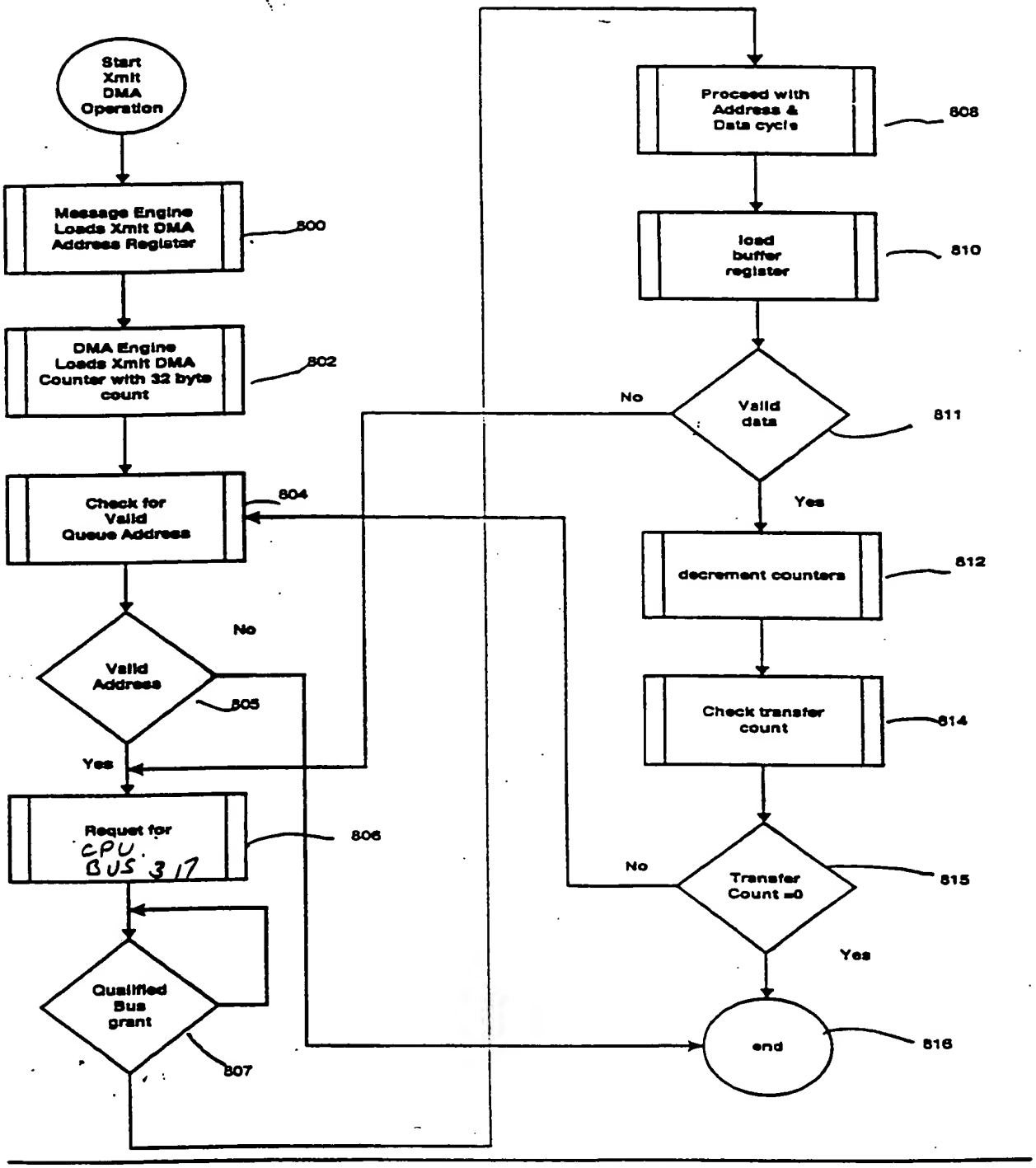


FIG 14B

Xmit Msg fl w

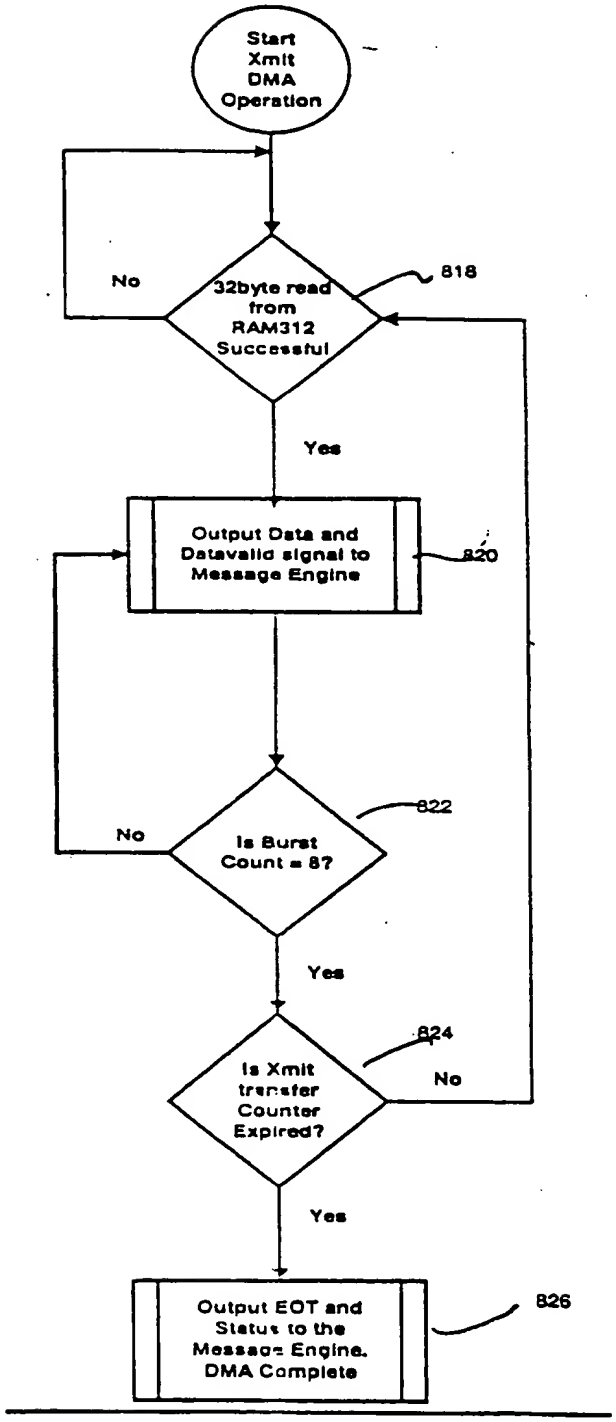


FIG 15A

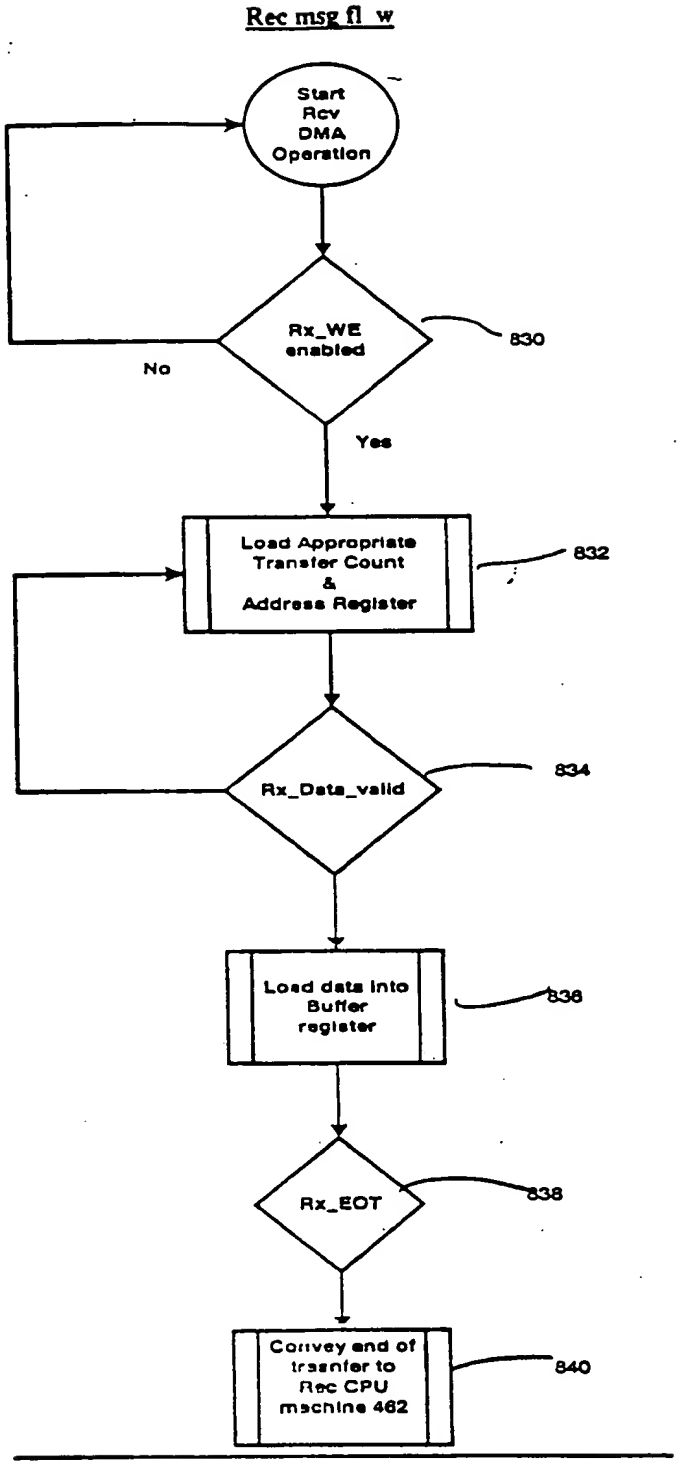

Rec msg fl w
Start Rcv DMA Operation
Rx_WE enabled
830
No
Yes
Load Appropriate Transfer Count & Address Register
832
Rx_Data_valid
834
Load data into Buffer register
836
Rx_EOT
838
Convey end of transfer to Rec CPU machine 462
840

FIG 15B

Rec cpu flow